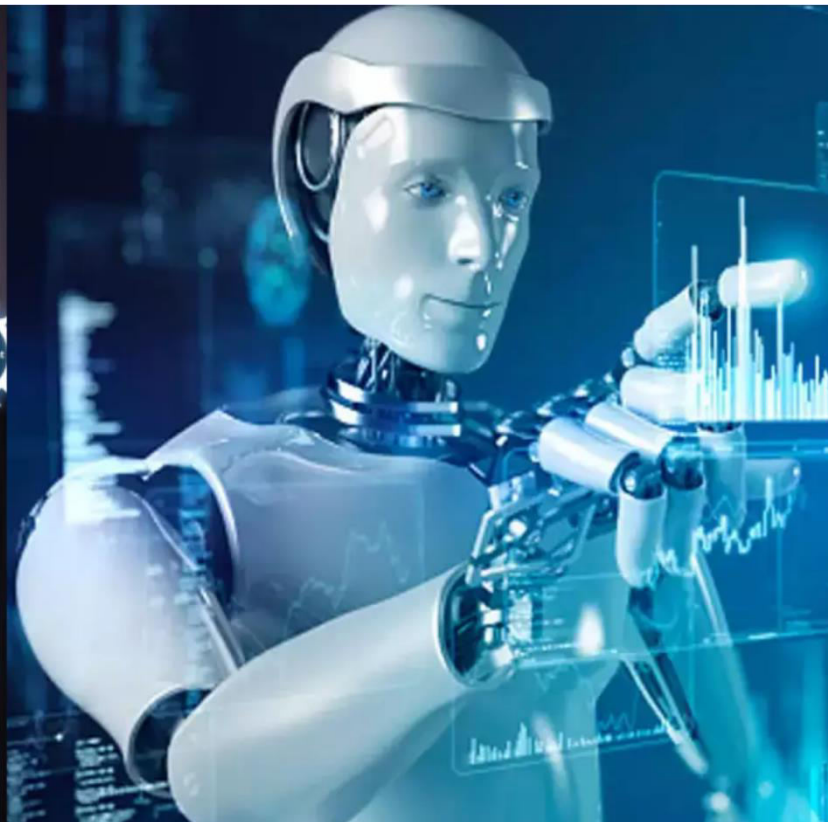




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Design and Implementation of a 32-Bit MIPS RISC Processor with Flexible 7 Stage Pipelining and Dynamic Thermal Control with Verilog System

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ABSTRACT: This paper presents the design and implementation of a **32-bit MIPS RISC processor** with a **flexible 7-stage pipelining** and **dynamic thermal control** mechanism. The processor follows the MIPS architecture, which is widely used in embedded and high-performance computing applications. The **flexible 7-stage pipeline** allows optimization of execution speed and power consumption by dynamically adjusting the pipeline depth based on workload and performance requirements. The **dynamic thermal control mechanism** is implemented to monitor temperature variations and adjust clock frequency or pipeline depth to prevent thermal hotspots, ensuring reliability and energy efficiency. The design is implemented using **Verilog** and verified using **System Verilog**, with FPGA-based synthesis and performance analysis conducted to evaluate execution efficiency, power consumption, and thermal management. The results demonstrate that the processor achieves improved throughput while maintaining optimal power and thermal performance.

KEYWORDS: RISC, CISC, MIPS, ALU, ISA

I. INTRODUCTION

The design and implementation of high-performance processors are pivotal in modern computing systems, where speed, flexibility, and efficiency are paramount. This project focuses on the development of a 32-bit MIPS (Microprocessor without Interlocked Pipeline Stages) RISC (Reduced Instruction Set Computer) processor incorporating a flexible 7-stage pipeline architecture. MIPS architecture, known for its simplicity and efficiency, serves as an ideal foundation for exploring pipeline techniques in processor design.

Traditional 5-stage pipelined MIPS architectures, although effective, face limitations in instruction throughput and performance at higher clock frequencies. To overcome these limitations, the proposed design extends the conventional pipeline to 7 stages, effectively enhancing instruction-level parallelism while minimizing hazards and bottlenecks. The additional stages in the pipeline are strategically introduced to optimize instruction fetch, decode, execution, memory access, and write-back processes.

This extended pipelining approach enables better control of data, structural, and control hazards, improving the overall performance of the processor. By splitting certain stages such as instruction decode and execution into finer stages, clock cycle duration can be reduced, allowing the processor to operate at higher clock frequencies without compromising correctness. This leads to significant performance gains, especially in systems demanding high-speed computation.

II. PROPOSED SYSTEM

The 7-stage pipelined RISC-V processor architecture builds upon the traditional 5-stage pipeline by further splitting critical stages to enhance processing speed and balance workload across the pipeline. This extended design includes the following stages: Instruction Fetch (IF), Instruction Decode (ID), Execute 1 (EX1), Execute 2 (EX2), Memory Address

(MEM1), Memory Access (MEM2), and Write Back (WB). The IF stage is responsible for fetching the instruction from the Instruction Memory using the Program Counter (PC). The PC updates sequentially or conditionally through a branch decision mechanism, driven by control signals and branch condition evaluators. In the ID stage, the fetched instruction is decoded, control signals are generated, and the register file is accessed to read the source operands. The instruction's immediate value, if present, is extracted and sign-extended to align with operand widths.

The execution phase is split into two stages: EX1 handles preliminary operations such as operand forwarding, branch comparison, and early ALU calculations. This stage also determines if a branch is taken, allowing the pipeline to resolve branches earlier and reduce misprediction penalties. EX2 completes the main ALU operation, such as addition, subtraction, or logic computations, and prepares memory addresses for load/store operations. Splitting the execution phase reduces the critical path, making timing closure easier at higher frequencies.

The MEM1 stage calculates the effective memory address and performs boundary or alignment checks, while MEM2 carries out the actual memory read or write operation, depending on whether it's a load or store instruction. Splitting memory access into two phases accommodates memory timing delays and supports integration with more complex memory systems like cache or multi-ported memory arrays. Finally, the WB (Write Back) stage updates the destination register in the register file with either the result from the ALU or the data retrieved from memory, depending on the instruction type.

Throughout the pipeline, control units and multiplexers govern the flow of data and decisions, including forwarding, hazard detection, and selection logic. By dividing execution and memory access into two separate stages each, the 7-stage pipeline achieves better clock frequency performance, smoother timing, and enhanced instruction throughput. This architecture is especially suitable for high-speed embedded processors or processors with multi-issue capabilities that demand optimized data paths without excessive logic per cycle.

A custom RISC processor typically follows a streamlined architecture designed for simplicity, efficiency, and speed. Its core components include the Instruction Memory, where program instructions are stored, and the Program Counter (PC), which keeps track of the current instruction address. The processor operates in several stages: Instruction Fetch (IF) retrieves the instruction from memory; Instruction Decode (ID) interprets the instruction and accesses the required data from the Register File. The Execute (EX) stage performs operations using the ALU (Arithmetic Logic Unit), such as arithmetic or logic functions. If needed, the Memory (MEM) stage accesses Data Memory for load or store instructions. Finally, the Write Back (WB) stage stores the result back into the register file. A Control Unit coordinates all these operations by generating appropriate control signals. This modular and pipelined design allows RISC processors to execute instructions efficiently and is widely used in embedded systems and custom hardware solutions

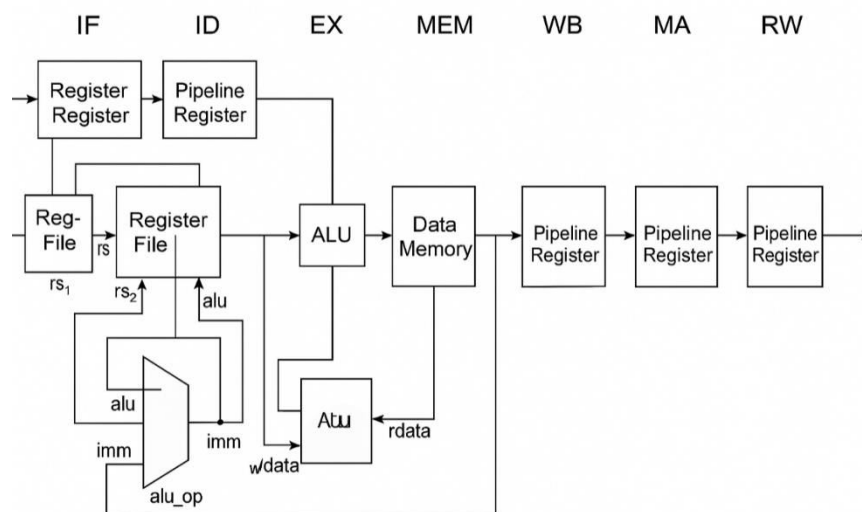


Fig. 1: Architecture of 7-stage pipelining

III. EXPERIMENTAL RESULTS

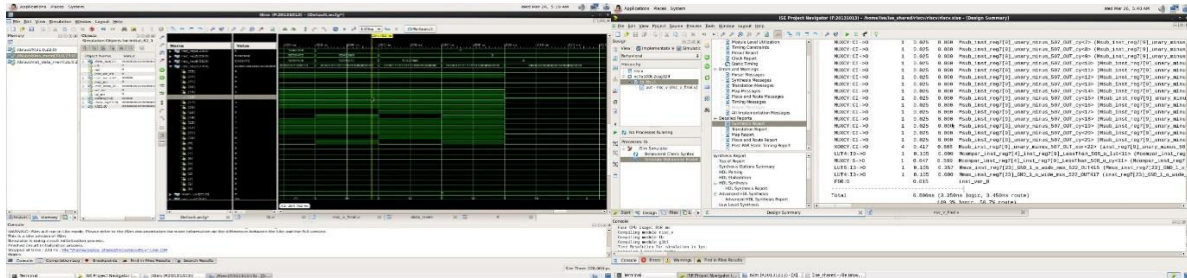


Fig. 1: Output waveform Fig 3: Timing Analysis

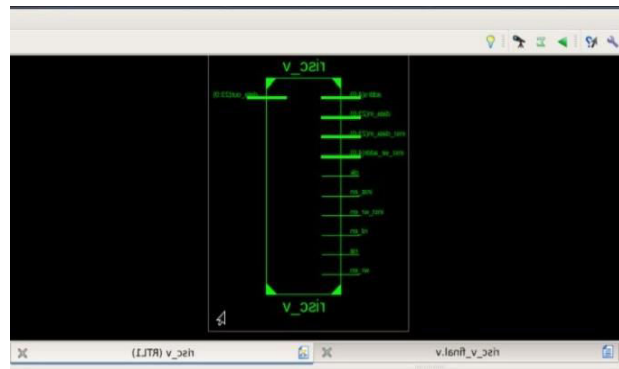
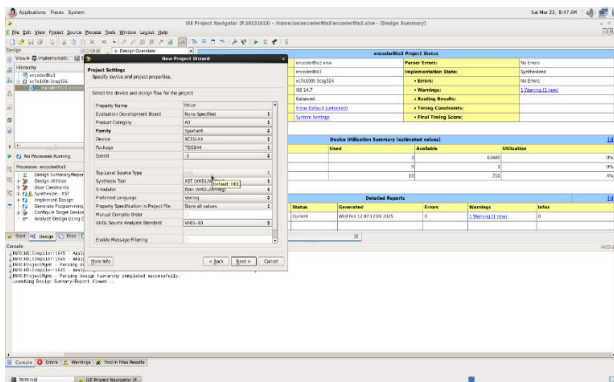


Fig. 2: Summary of Area Fig. 4: RISC_V RTL

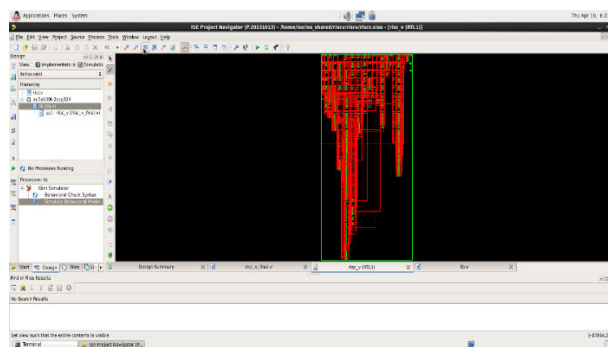


Fig. 5: Internal RTL of module

IV. CONCLUSION

The implementation of a 32-bit MIPS RISC processor with a flexible 7-stage pipelining and dynamic thermal control enhances performance, power efficiency, and thermal stability. The flexible pipeline architecture provides adaptability to various computing needs, while thermal management techniques ensure optimal operation under different workloads. FPGA-based synthesis and testing validate the design’s feasibility, showing improved execution efficiency and lower thermal stress. This work demonstrates that dynamic pipeline management and thermal-aware processing can significantly enhance processor performance and reliability.

REFERENCES

- [1] Andrew Waterman, Krste Asanovi, and Five Inc. "The RISC-V Instruction Set Manual Volume I: User Level ISA Document Version 2." CS Division, EECS Department, University of California, Berkeley 2017.
- [2] David A. Patterson and John L. Hennessy "Computer Organization and Design RISC-V Edition: The Hardware Software Interface." Morgan Kaufmann Publishers Inc., 2017, San Francisco, CA, USA.
- [3] Ludovico Poli, Sangeet Saha, Xiaojun Zhai and Klaus D. McDonald- Maier, "Design and Implementation of a RISC V Processor on FPGA" 17th International Conference on Mobility, Sensing and Networking (MSN)
- [4] Don Kurian Dennis, Ayushi Priyam, Sukhpreet Singh Virk, Sajal Agrawal, Tanuj Sharma, Arijit Mondal and Kailash Chandra Ray, "Single Cycle RISC-V Micro Architecture Processor and its FPGA Prototype", Seventh International Symposium on Embedded Computing and System Design (ISED), Durgapur, India, 2017, pp. 1- 5, doi: 10.1109/ISED.2017.8303926.
- [5] Wendi Zhang, Yonghui Zhang and Kun Zhao, "Design and Verification of Three-stage Pipeline CPU Based on RISC-V Architecture" 5th Asian Conference on Artificial Intelligence Technology (ACAIT) 2021.
- [6] P. Singh, A. Rai, A. Rajput, P. C. Joshi and A. Prakash, "Design and Analysis of High-Speed RISC Processor Using Pipelining Technique,"2022 4th International Conference on Advances in Computing, Communication Control and Networking (ICAC3N), Greater Noida, India, 2022, pp. 1642-1645, doi: 10.1109/ICAC3N56670.2022.10074423.
- [7] J. Jeemon, "Pipelined 8-bit RISC processor design using Verilog HDL on FPGA," 2016 IEEE International Conference on Recent Trends in Electronics, Information & Communication Technology (RTEICT), Bangalore, India, 2016, pp. 2023-2027, doi: 10.1109/RTEICT.2016.7808194.
- [8] S. Prabhakaran, M. N and V. Vedanarayanan, "Design and Analysis of a Multi Clocked Pipelined Processor Based on RISC-V," 2022 International Conference on Communication, Computing and Internet of Things (IC3IoT), Chennai, India, 2022, pp. 1-5, doi: 10.1109/IC3IOT53935.2022.9767960.
- [9] A. Tiwari, P. Guha, G. Trivedi, N. Gupta, N. Jayaraj and J. Pidanic, "IndiRA: Design and Implementation of a Pipelined RISC-V Processor," 2023 33rd International Conference Radioelektronika (RADIOELEKTRONIKA), Pardubice, Czech Republic, 2023, pp. 1-6, doi: 10.1109/RADIOELEKTRONIKA57919.2023.10109058.
- [10] I. Thanga Dharsni, K. S. Pande and M. K. Panda, "Optimized Hazard Free Pipelined Architecture Block for RV32I RISC-V Processor," 2022 3rd International Conference on Smart Electronics and Communication (ICOSEC), Trichy, India, 2022, pp. 739-746, doi: 10.1109/ICOSEC54921.2022.9952122.



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