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Comparative Performance Analysis of MTCMOS-Based Combinational Logic Circuits for Low-Power Applications

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ABSTRACT: Efficient power management is a critical aspect of electronic systems, significantly influencing the evolution of modern technology. In modern electronic systems, power consumption plays a crucial role in determining performance, efficiency, and sustainability. Multi-Threshold Complementary Metal-Oxide-Semiconductor (MTCMOS) technology has emerged as a promising solution for reducing leakage power while maintaining circuit performance. This paper presents a comparative analysis of various MTCMOS-based combinational logic circuits, evaluating their effectiveness in terms of power dissipation, propagation delay, and overall performance. The study involves simulations of key combinational circuits, such as logic gates, multiplexers, and arithmetic units, under different operating conditions. Results demonstrate the trade-offs between power savings and speed in MTCMOS implementations, highlighting the optimal design choices for low-power applications. The findings contribute to the development of energy-efficient digital circuits, making MTCMOS a viable candidate for next-generation low-power VLSI designs.

KEYWORDS: Multi - Threshold Complementary Metal – Oxide – Semiconductor (MTCMOS), Combinational Logic Circuits, Power dissipation, Propagation delay, Low Power VLSI design.

I. INTRODUCTION

As the number of gates per chip continues to increase with higher levels of integration, the power requirements of computer systems also rise proportionally. Over the past decade, energy budget considerations and their analysis have played a crucial role in system architecture design. Number of useful techniques have been demonstrated to mitigate power consumption. This research addresses the pressing challenge of power consumption within the combinational logic circuits and proposes a novel approach for substantial power optimization.

Maram Ashok et al. [1] proposed a deep genetic mechanism for power prediction in high-speed VLSI adder circuits. Their study analyzes power optimization techniques to enhance efficiency. Sai Surendra et al. [2] explored the design and implementation of a low-power adder circuit using the LECTOR technique. The proposed method demonstrates effective leakage power reduction while maintaining circuit performance. The results highlight the potential of LECTOR-based designs for energy-efficient VLSI applications. This work contributes to advancing low-power digital circuit methodologies.

Ketan J. Raut et al. [3] examined various modern optimization techniques for reducing power dissipation, highlighting adiabatic logic design and asynchronous computation as promising approaches. However, the study includes those practical limitations related with these techniques, indicating challenges in their widespread implementation.

Kalpana K. et al. [4] investigated the design and performance analysis of low-power, high-speed adders and multipliers using MTCMOS across 90nm, 70nm, 25nm, and 18nm technologies. The developed method examines power and speed trade-offs in scaling regimes. The results demonstrate MTCMOS's effectiveness in reducing power consumption while maintaining performance. This research supports MTCMOS as a viable solution for energy-efficient VLSI design.

Anusha Kondamet al.[5] proposed a low-power clocking system for D-flip flops using MTCMOS and the Slumber Keeper technique. The study highlights significant reductions in power consumption while maintaining performance and findings demonstrate the effectiveness of these techniques in low-power sequential circuit design. Mayank Chakraverty et al. [6] discussed about the architectural and logic level power optimization techniques for low power consumption.

Kamal K. Mehta et al.[7] reviewed various strategies and methodologies for dynamic power reduction in low-power system design. They explored various techniques to optimize power consumption without compromising performance. The findings emphasize efficient power management approaches for modern VLSI circuits. J. Caroline Bonpapa et al.[8], explained the simulation of three different types of multipliers and compared using 32nm Berkeley Predictive Technology Model (BPTM) between MOSFET 32nm and CNTFET 32nm technology. The multiplier which has designed using CNFET reduces 99% of power compared to MOSFET. Among all the three different multipliers the Vedic multiplier proves to be the best compared with the array and Wallace multiplier.

Esther Rani Thuraka et al. [9] explored high-performance ALU design using MTCMOS, Enhanced MTCMOS (EMTCMOS), and transistor stacking techniques. Their study highlights power gating and transistor stacking for significant leakage reduction and the results demonstrate that EMTCMOS further minimizes leakage over conventional MTCMOS with minimal delay. Several studies have explored strategies, methodologies, and power management techniques for low-power circuit and system design[10,11].

The output of proposed approach is empirically validated, positioning it as a promising solution for low-power applications across a diverse spectrum of electronic devices and systems. In this pursuit of power optimization, the outcomes of this research promise to shape the future of energy-efficient electronic systems, paving the way for sustainable and high-performance technology.

II. METHODOLOGY

NAND Transistor

The NAND gate is a fundamental building block in digital logic circuits, widely used in combinational and sequential logic design. It is implemented using complementary MOS (CMOS) technology, where a series-parallel configuration of nMOS and pMOS transistors determines its operation. In a conventional CMOS NAND gate, pMOS transistors are connected in parallel, and nMOS transistors are in series, ensuring low power dissipation and high noise margins. However, as device scaling progresses, leakage power becomes a major concern, necessitating advanced power reduction techniques.

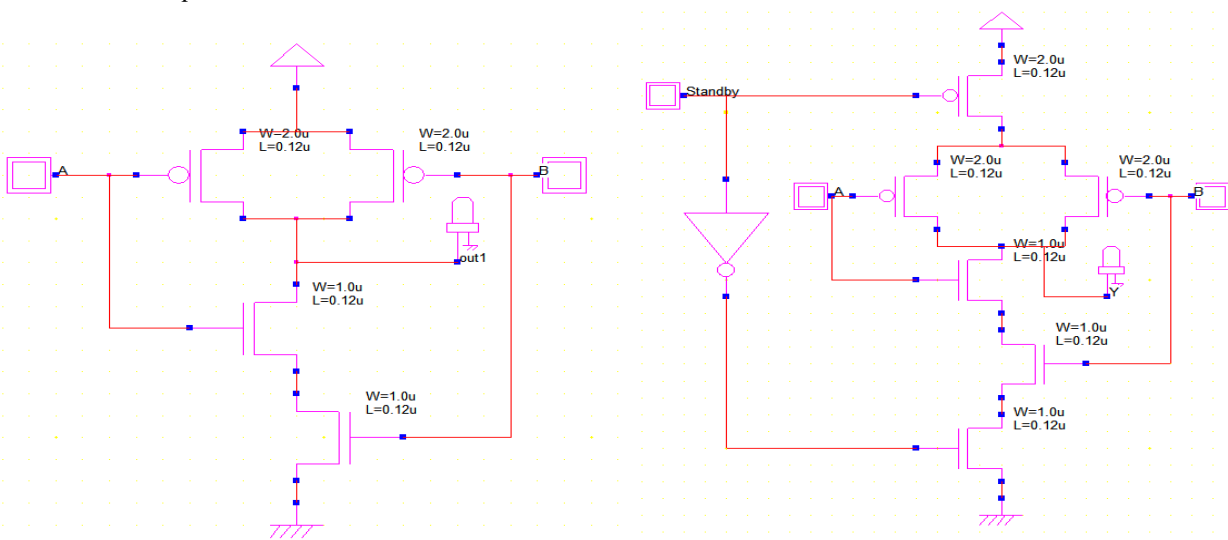


Figure 1. (a). NAND Transistor and (b).MTCMOS NAND

MTCMOS NAND

Multi-Threshold CMOS (MTCMOS) technology is an effective approach to reducing leakage power in digital circuits while maintaining performance. An MTCMOS NAND gate integrates high-threshold voltage (HVT) and low-threshold voltage (LVT) transistors to optimize power and speed. HVT transistors act as sleep transistors, disconnecting the circuit from the power supply during idle states, thereby reducing leakage. The implementation of MTCMOS in NAND gates significantly reduces static power dissipation while maintaining dynamic performance. This technique is crucial for energy-efficient VLSI design, particularly in low-power applications such as mobile and embedded systems.

NOR Transistor

The NOR gate is a fundamental digital logic gate widely used in combinational and sequential circuits. It is implemented using CMOS (Complementary Metal-Oxide-Semiconductor) technology, where pMOS transistors are connected in series, and nMOS transistors are in parallel. The NOR gate produces a high output only when all inputs are low; otherwise, the output remains low. Due to its universal nature, NOR gates are extensively used in memory design, arithmetic circuits, and control logic. However, with increasing transistor miniaturization, leakage power dissipation has become a significant issue, necessitating the adoption of advanced low-power techniques.

MTCMOS NOR

Multi-Threshold CMOS (MTCMOS) technology is a well-established approach to mitigating leakage power in digital circuits while maintaining performance. An MTCMOS NOR gate integrates both high-threshold voltage (HVT) and low-threshold voltage (LVT) transistors, where HVT transistors serve as sleep transistors to disconnect the power supply during inactive states. This effectively reduces static power dissipation while preserving the circuit's dynamic response. The application of MTCMOS in NOR gates help to achieve significant energy savings, making it a suitable technique for low-power VLSI designs, particularly in mobile, embedded, and high-performance computing applications.

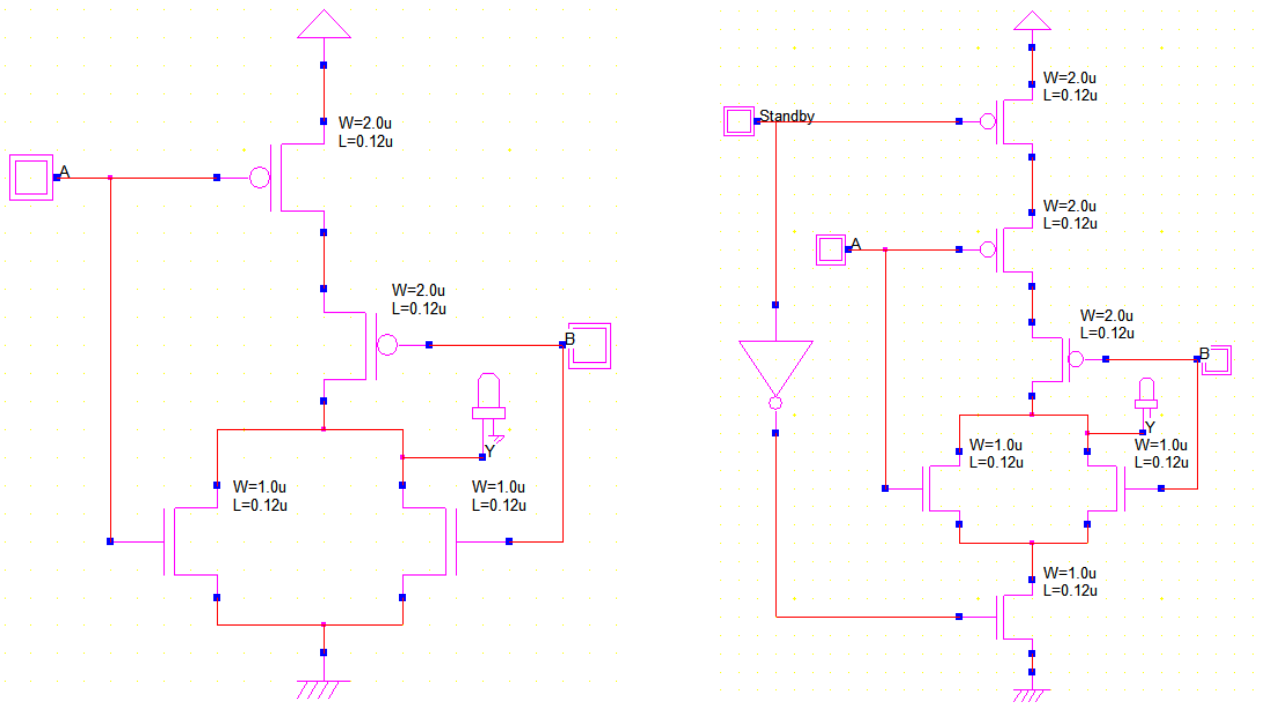


Figure 2.(a). NOR Transistor and (b).MTCMOS NOR

III. RESULTS AND DISCUSSION

In this, simulation method conducted using Microwind and DSCH tool, a conventional NAND and NOR, MTCMOS NAND and NOR were constructed as given in the Figure 1 & 2. The output simulation of NAND, MTCMOS NAND and NOR, MTCMOS NOR were shown in Figure 3 & 6. To evaluate the performance of the power consumption, layout for the NAND and NOR has generated as shown in the Figure 4 & 7. Layout Schematic Diagram for NAND Transistor & MTCMOS NAND, NOR Transistor & MTCMOS NOR were shown in Figure 5 & 8.

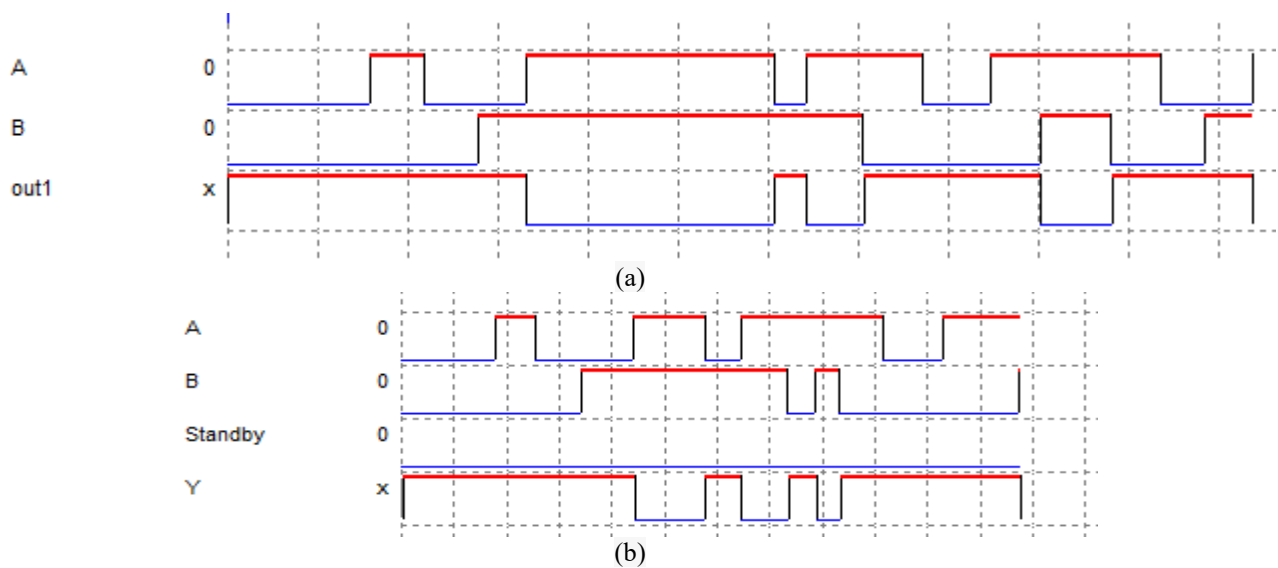
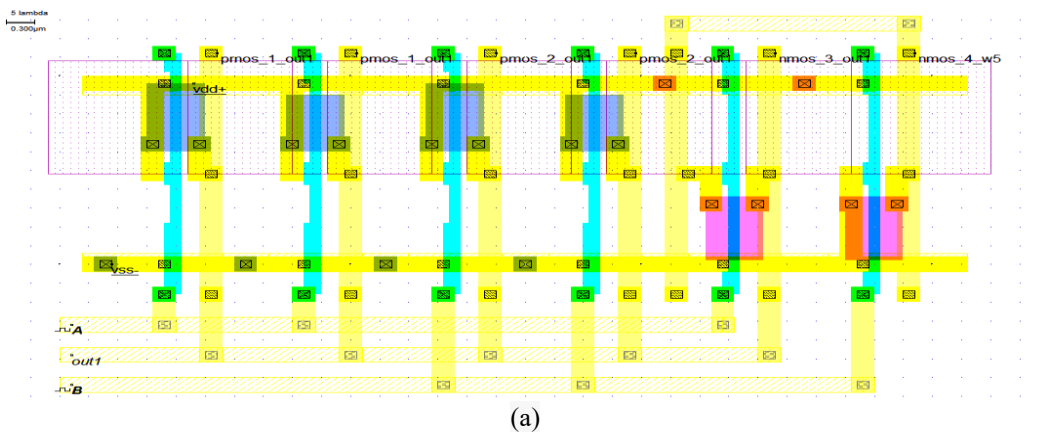
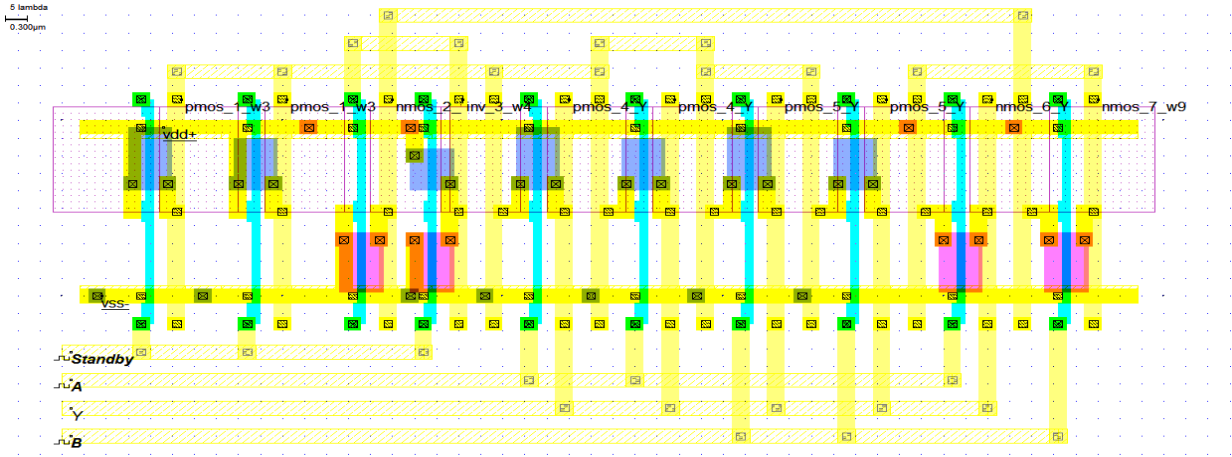


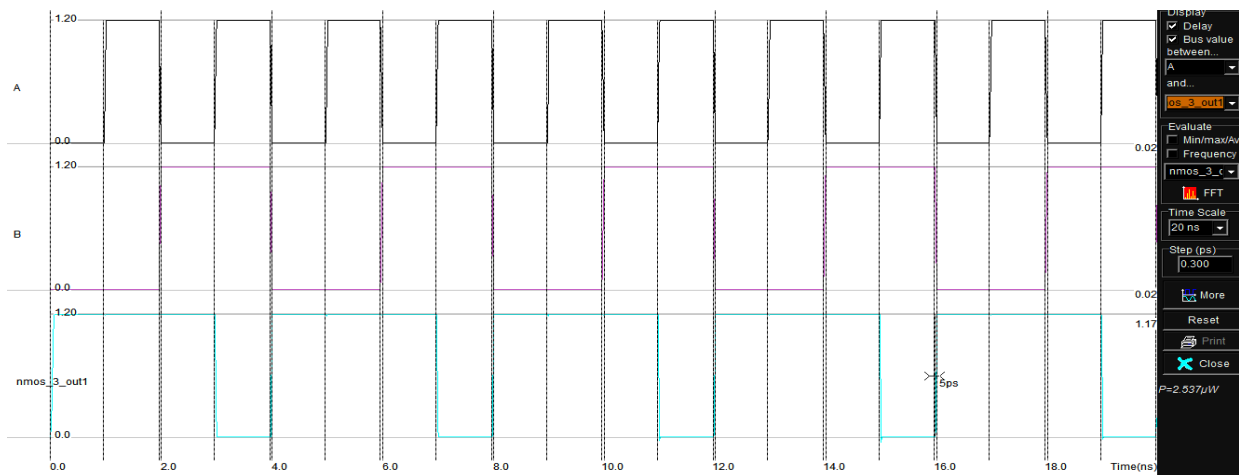
Figure.3. (a) Simulated output of NAND Transistor (b) Simulated output of MTCMOS NAND



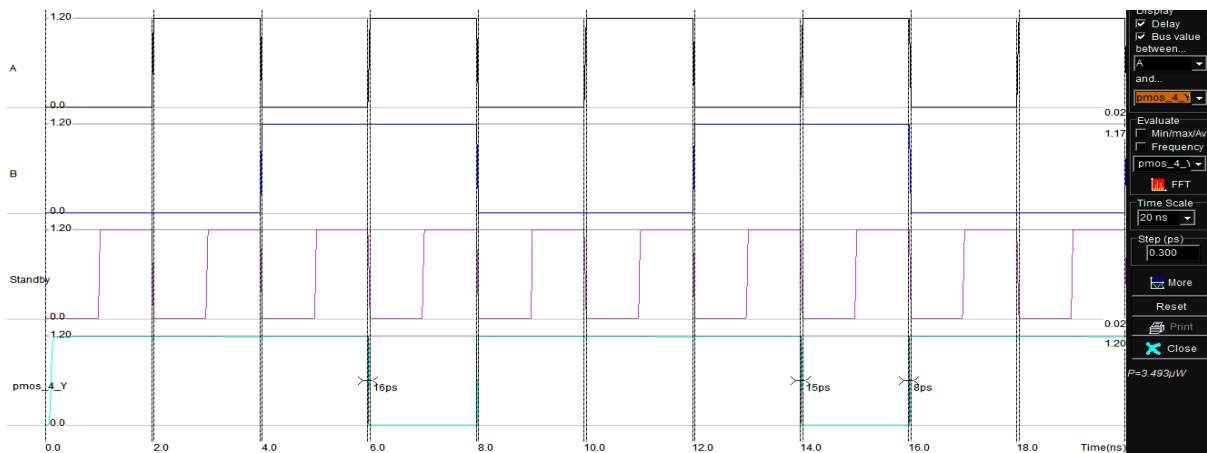


(b)

Figure.4. Layout Diagram for NAND Transistor(b) Layout Diagram for MTCMOS NAND



(a)



(b)

Figure.5. Layout Schematic Diagram for NAND Transistor (b) Layout Schematic Diagram for NAND MTCMOS

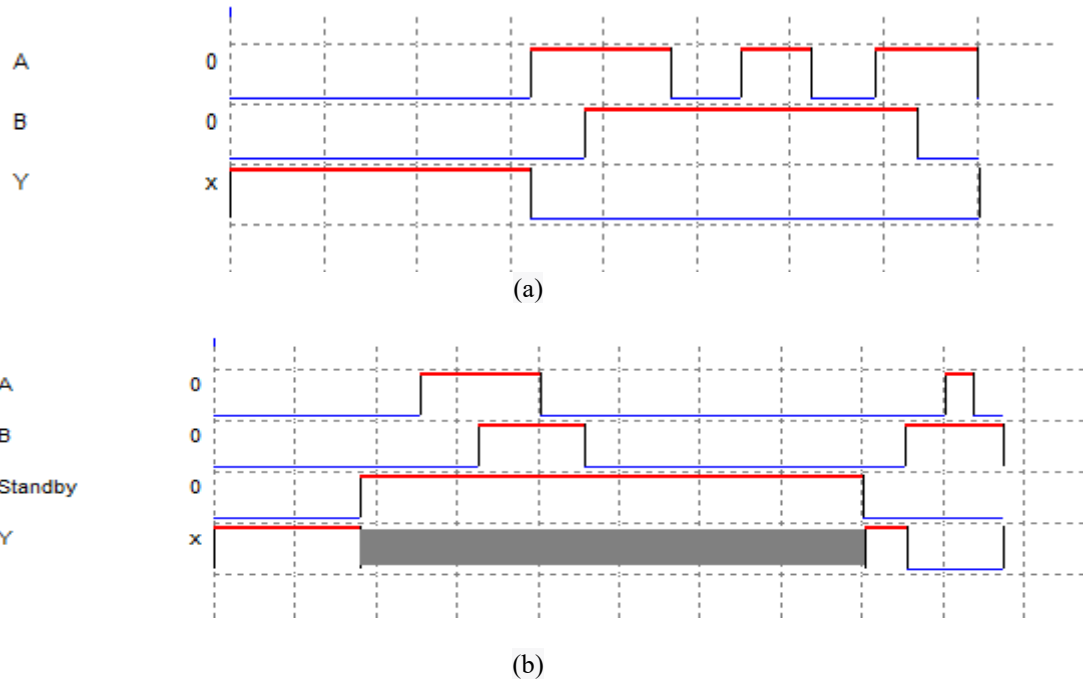
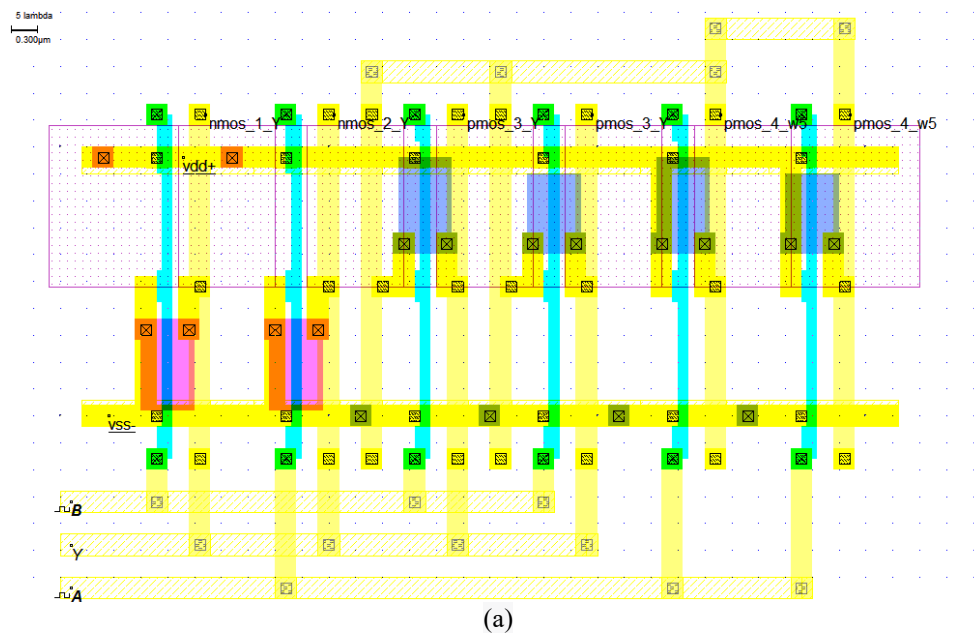


Figure.6. (a) Simulated output of NOR Transistor (b) Simulated output of MTCMOS NOR



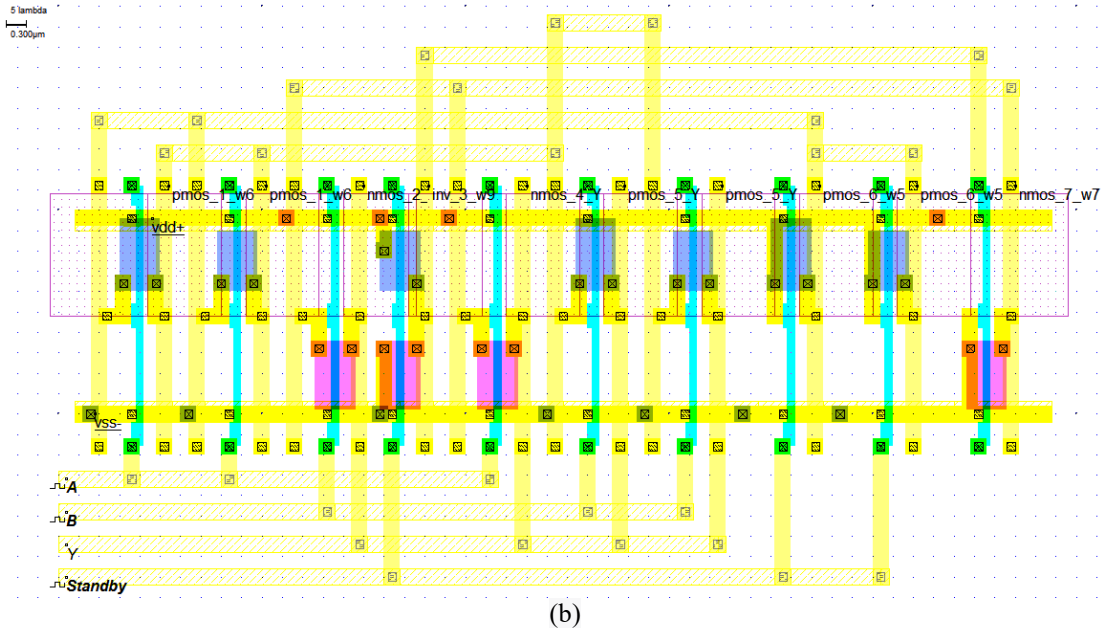
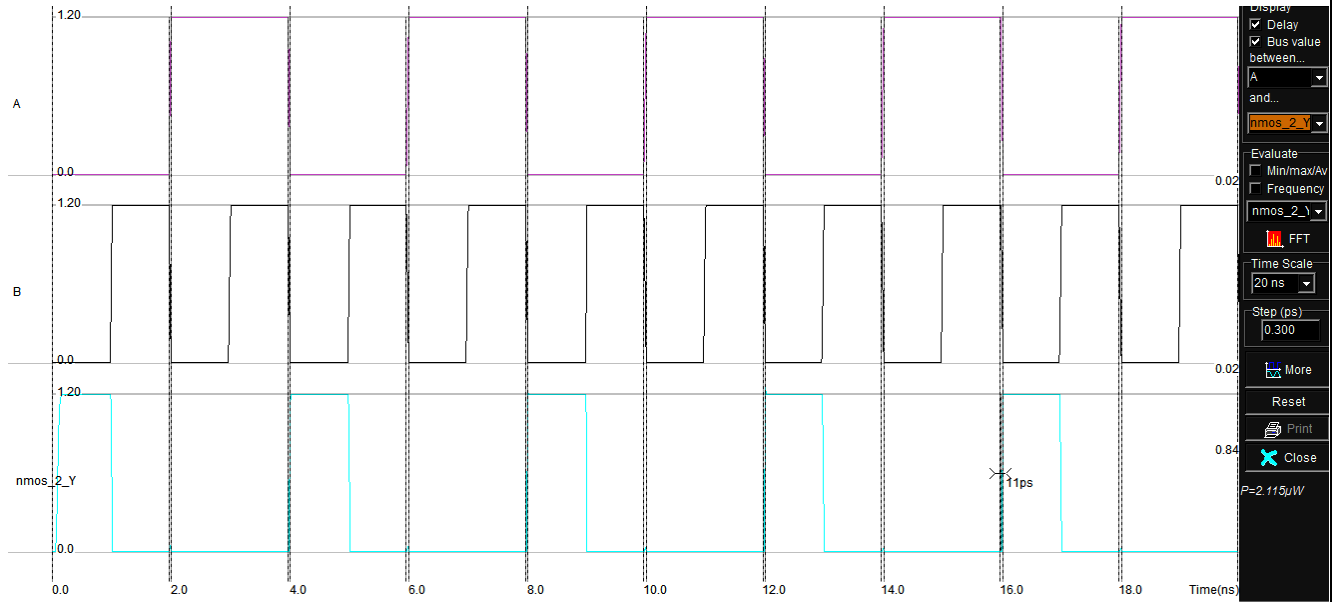


Figure.7.(a) Layout Diagram for NOR Transistor (b) Layout Diagram for MTCMOS NOR



(a)

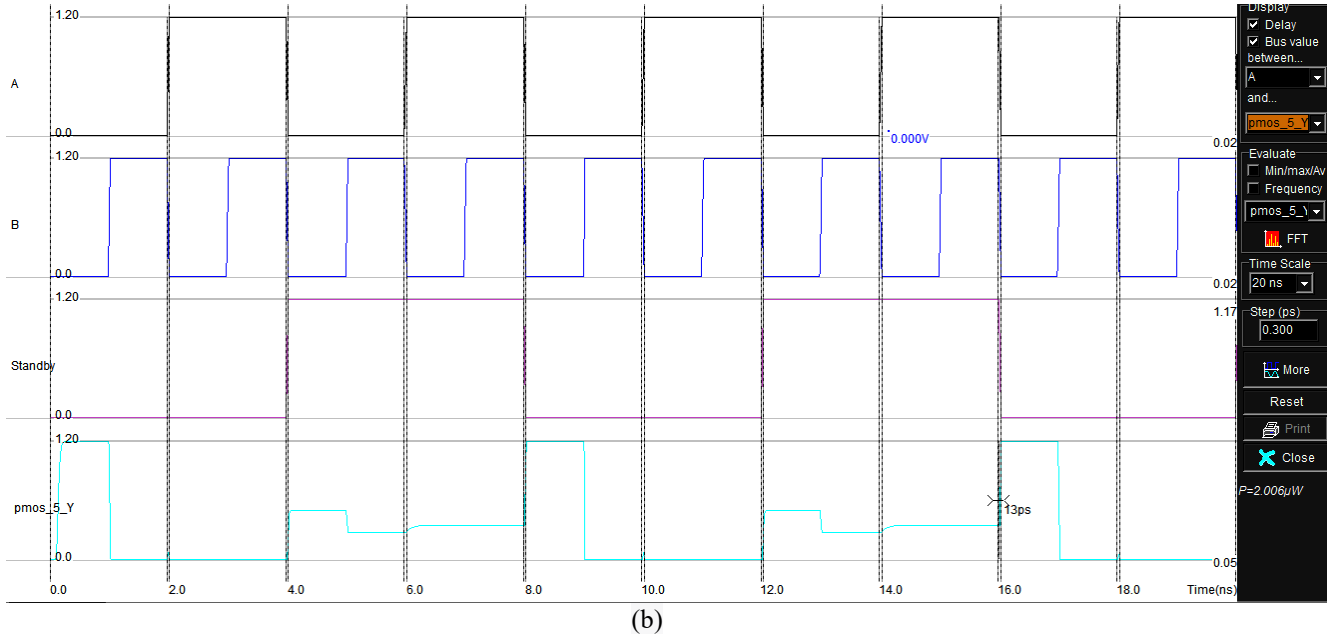


Figure.8.(a) Layout Schematic Diagram for NOR Transistor (b) Layout Schematic Diagram for NOR MTCMOS

The table.1 presents a comparative analysis of power dissipation in conventional NAND and NOR gates versus their MTCMOS counterparts. The conventional NAND gate exhibits a power dissipation of $2.537 \mu W$, whereas the MTCMOS NAND gate shows a reduced dissipation of $2.193 \mu W$ highlighting the effectiveness of MTCMOS in lowering power consumption. Similarly, the conventional NOR gate records a power dissipation of 2.115 units, which decreases to $2.006 \mu W$ with MTCMOS implementation.

This reduction in power dissipation demonstrates the efficiency of MTCMOS technology in minimizing leakage power while maintaining circuit performance, making it a suitable approach for low-power VLSI design.

Logic Circuits	Power Dissipated (μW)
Conventional NAND Transistor	2.537
MTCMOS NAND	2.193
Conventional NOR Transistor	2.115
MTCMOS NOR	2.006

Table.1. Comparison of NAND, MTCMOS NAND, NOR and MTCMOS NOR Power dissipation

IV. CONCLUSION

Efficient power management remains a crucial factor in the advancement of modern electronic systems, directly impacting performance, efficiency, and sustainability. This study conducted a comparative analysis of various MTCMOS-based combinational logic circuits, evaluating their power dissipation, propagation delay, and overall performance. Through simulations of key circuits, including logic gates, multiplexers, and arithmetic units, the results

highlight the trade-offs between power savings and speed in MTCMOS implementations. The findings provide valuable insights into optimal design choices for low-power applications, reinforcing the potential of MTCMOS technology in next-generation VLSI designs aimed at energy-efficient digital circuits. By addressing power consumption challenges without compromising operational integrity, this approach contributes to the advancement of energy-efficient electronic solutions. Future enhance research may explore further optimizations and adaptations to enhance power savings across a broader range of digital circuit applications.

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