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Design of Approximate Multipliers using Approximate Higher-Order Compressors

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ABSTRACT: The abstract presents a novel high-performance, 8:2 high-order compressor-based multiplication architecture designed to enhance computational efficiency in digital systems. It addresses the limitations of traditional multipliers, which often suffer from high power consumption, latency, and area constraints. By utilizing high-order compressors for partial product reduction, the architecture significantly minimizes the number of summation stages, thereby reducing propagation delay and improving speed. Extensive simulations and hardware implementations demonstrate that this architecture outperforms conventional multipliers in terms of speed and power efficiency, making it suitable for applications in high-performance computing, artificial intelligence, and digital signal processing. The design also emphasizes scalability and energy efficiency, positioning it as a leading solution for modern digital arithmetic challenges. By leveraging an efficient compressor-based carry propagation technique, the architecture improves latency, throughput, and energy efficiency, making it ideal for real-time computing applications.

KEYWORDS: High-Order Compressor, Multiplication Architecture, Partial Product Reduction, Verilog HDL, High-Performance Computing, Low Power Design.

I. INTRODUCTION

Multiplication is a fundamental operation in digital computing, critical to high-performance domains such as DSP, AI, cryptography, and image processing. Traditional multiplier architectures—like array, Wallace tree, and Booth multipliers—face limitations due to high latency and power inefficiency caused by excessive partial product summation and complex carry propagation. To address these challenges, this paper introduces a novel high-performance multiplication architecture based on an 8:2 high-order compressor. Unlike conventional 3:2 and 4:2 compressors, the 8:2 compressor reduces more partial products in a single stage, significantly lowering the number of summation levels. This enhances computational speed, reduces propagation delay, and improves energy efficiency. The proposed architecture achieves a balanced power-delay-area (PDA) trade-off and is scalable for integration into FPGAs, ASICs, and SoCs. Optimizations at both the logic and transistor levels minimize switching activity and power dissipation. Simulation results using standard CMOS technology demonstrate superior performance over existing designs, including Wallace, Dadda, and Booth multipliers, in terms of speed, power consumption, and silicon area. Further enhancements are realized through hybrid carry strategies, power-gating, and clock-gating techniques, making the design ideal for real-time, low-power applications. Robustness under varying voltage and temperature conditions is validated through extensive testing. Comparative analysis highlights the design's superior energy-per-operation, throughput, and manufacturability. This architecture represents a scalable, energy-efficient solution for next-generation computing platforms, with strong potential in AI accelerators, machine learning hardware, and cryptographic processors. Future work will explore further logic optimizations and support for multi-precision arithmetic.

II. PROPOSED SYSTEM

A 16×16 multiplier using 8:2 compressors first generates 256 partial products by performing bitwise AND operations between each bit of the two 16-bit operands. These partial products form a matrix that is then reduced through a multi-stage compressor tree. In this tree, 8:2 compressors reduce the number of bits in each column by compressing eight input bits into three outputs (sum, carry, and carry-out), effectively minimizing the required addition stages. After the

reduction, only two rows (a sum row and a carry row) remain. These two rows are then added using a fast carry-propagate adder, such as a carry-lookahead adder, to produce the final 32-bit product. This architecture minimizes delay and hardware complexity by reducing the critical path in the partial product summation phase.

The proposed high-performance, 8:2 high-order compressor-based multiplication architecture is specifically designed to enhance computational efficiency by optimizing the partial product reduction process. The architecture consists of three primary stages: partial product generation, partial product reduction using high-order compressors, and final summation. In the first stage, partial products are generated using an optimized version of the traditional AND gate array structure, ensuring minimal signal propagation delay. Unlike conventional multipliers, where partial products are accumulated in multiple levels, the proposed architecture introduces a novel 8:2 compressor-based reduction technique, significantly decreasing the number of intermediate summation layers. The 8:2 compressor operates by taking eight input bits at a time and generating only two output bits—one sum bit and one carry bit—leading to a considerable reduction in logic depth and propagation delay. The logic formulation of the 8:2 compressor is designed to minimize the number of logic gates required for its implementation, thereby reducing power consumption while maintaining high-speed operation. The compressor utilizes a combination of XOR, AND, and multiplexer (MUX) circuits to efficiently compute the sum and carry outputs with minimal delay. Additionally, the proposed architecture employs an optimized carry propagation strategy to further enhance speed by ensuring that carry signals are efficiently transmitted across compressor blocks without introducing unnecessary latency.

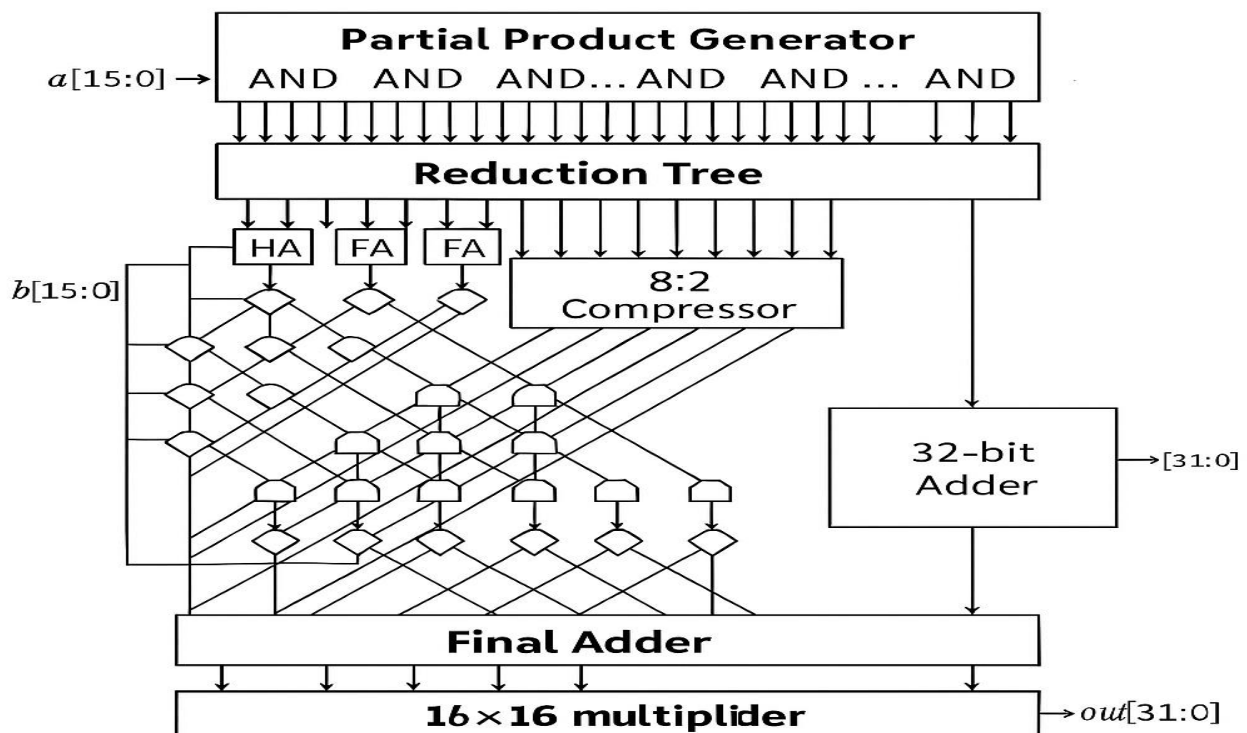


FIG 2: BLOCK DIAGRAM OF OPERARTION OF 16*16 MULTIPLIER USING 8:2 COMPRESSOR

The partial product reduction stage is the most crucial part of the architecture, as it determines the overall speed and efficiency of the multiplier. Traditional reduction methods, such as Wallace tree and Dadda approaches, rely on multiple levels of summation using 3:2 and 4:2 compressors, leading to increased circuit complexity and higher power dissipation. In contrast, the proposed 8:2 compressor-based reduction strategy significantly reduces the number of summation levels by compressing more bits in each stage. The compressor arrangement is optimized to minimize the number of logic transitions, reducing switching activity and thereby lowering dynamic power consumption. The interconnect structure between compressors is also carefully designed to minimize signal propagation delay, ensuring that critical path delays are kept to a minimum. This is particularly beneficial in deep-submicron CMOS technology

nodes, where interconnect delay becomes a major bottleneck in high-speed arithmetic circuits. Furthermore, to enhance the robustness of the architecture, a hybrid carry propagation approach is implemented, balancing between ripple-carry and carry-lookahead techniques to achieve an optimal trade-off between speed and power efficiency. The final summation stage employs an optimized adder circuit, such as a carry-save adder (CSA) or carry-select adder (CSeA), to compute the final product with minimal latency. The choice of the final adder depends on the target application and performance requirements, with carry-select adders being preferred for high-speed designs and carry-save adders offering better power efficiency. An **8:2 compressor** takes eight input bits and compresses them into three outputs: **Sum, Carry, and Cout** (carry-out to the next stage). It is built using **4 full adders, 6 AND gates, and 3 XOR gates**, allowing efficient parallel addition. This compressor helps reduce the number of partial products in multiplication. In the block diagram, the inputs are grouped and passed through logic gates to generate intermediate sums and carries. The final output combines these to produce the compressed result, improving speed and reducing hardware complexity.

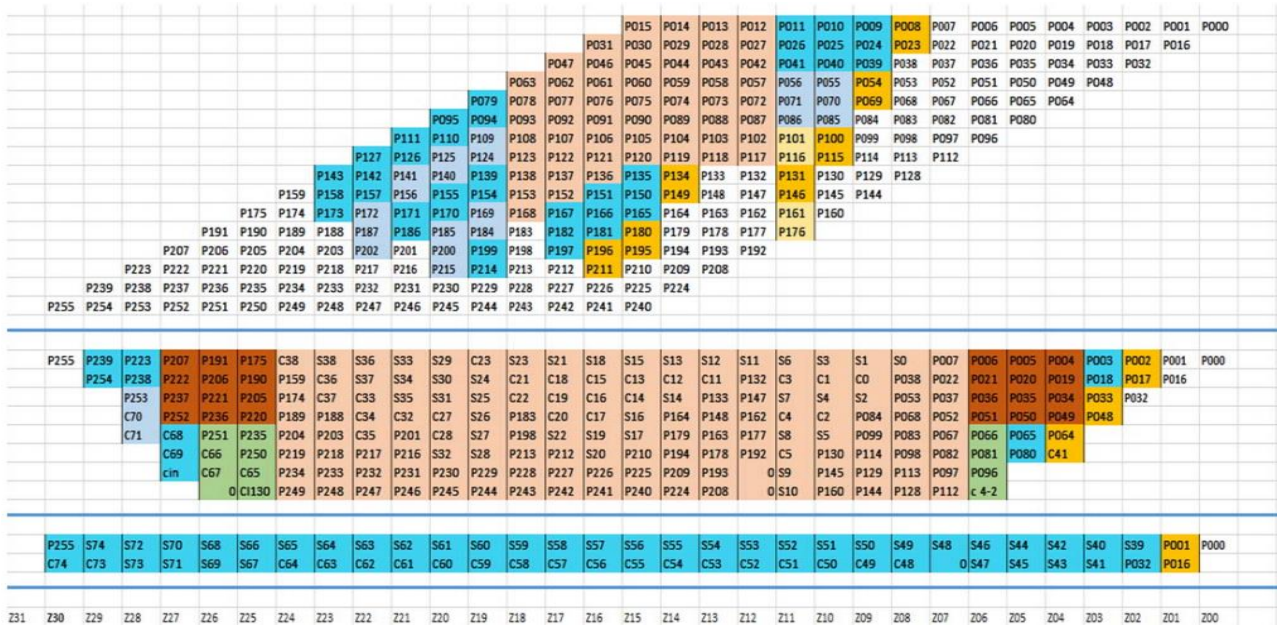


FIG 1: ARCHITECTURE OF 16*16 MULTIPLIER USING 8:2 COMPRESSOR

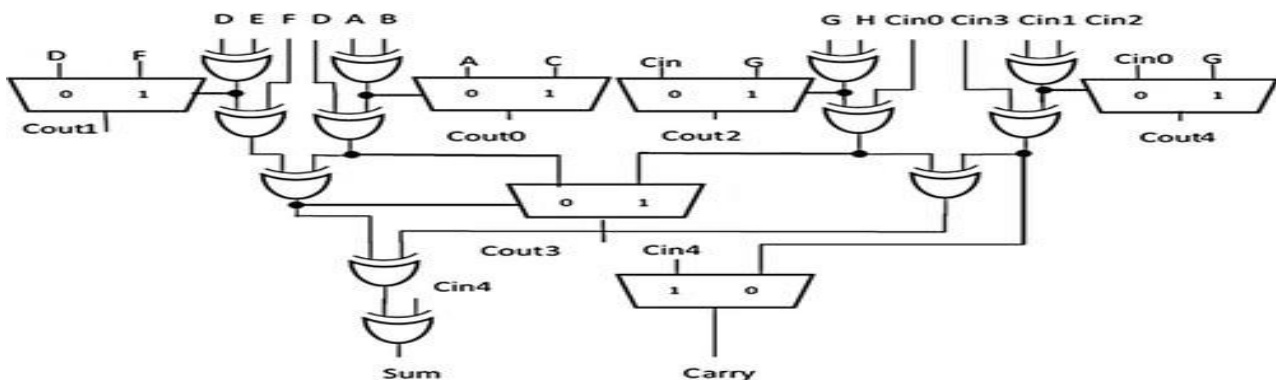


FIG 2: 8:2 COMPRESSOR ARCHITECTURE

The 8:2 compressor is a high-performance digital circuit architecture designed to efficiently reduce eight input bits and two carry inputs into two outputs—sum and carry—along with several intermediate carry outputs. It plays a crucial role in high-speed multiplication architectures by significantly minimizing the number of summation stages required for

partial product reduction. The architecture, as illustrated, uses a combination of XOR gates and multiplexers to process input bits in parallel, thereby generating intermediate carries (Cout0 to Cout4) that facilitate faster and more efficient carry propagation. The core advantage of the 8:2 compressor lies in its ability to handle a large number of inputs in a single computation stage, which drastically reduces delay and power consumption compared to traditional compressor designs such as 3:2 and 4:2 compressors. By reducing the critical path and optimizing logic-level operations, the 8:2 compressor enhances the overall throughput and energy efficiency of digital multipliers. This makes it especially suitable for applications requiring high-speed and low-power computation, such as digital signal processing, cryptographic systems, and AI accelerators. The architecture is scalable and can be seamlessly integrated into complex processing systems like FPGAs, ASICs, and SoCs, making it a valuable component in modern digital arithmetic designs.

III. EXPERIMENTAL RESULTS

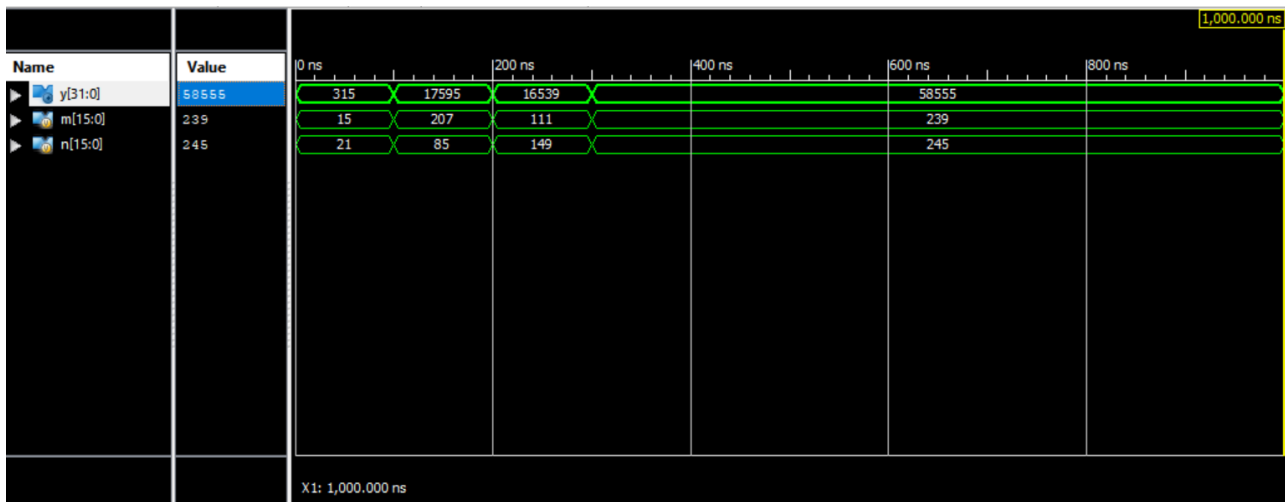


Fig 1: SIMULATION RESULT

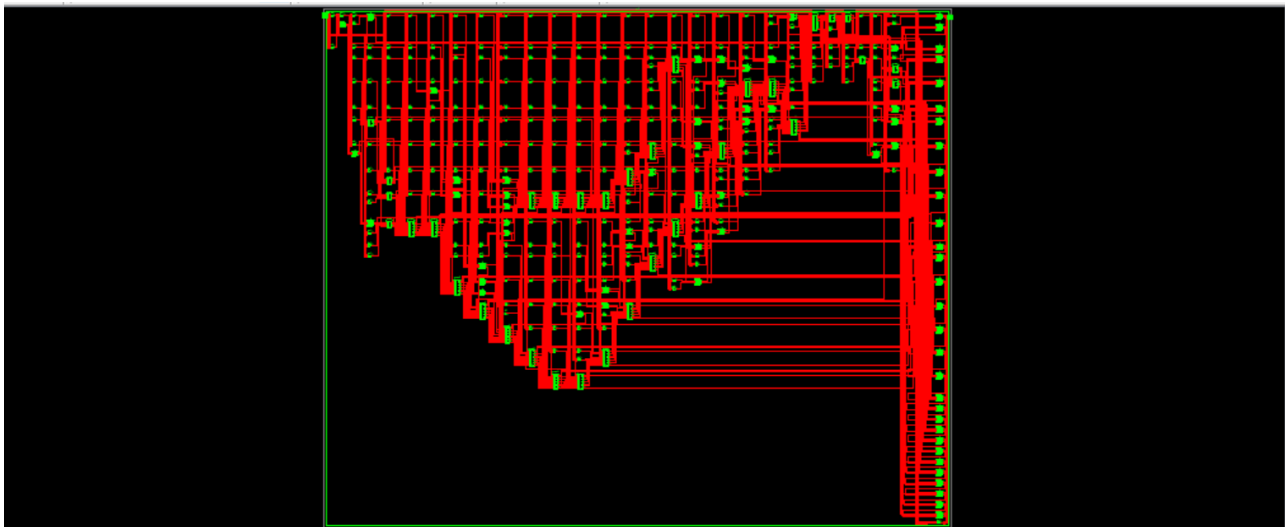


Fig 2: SYNTHESIS RESULT

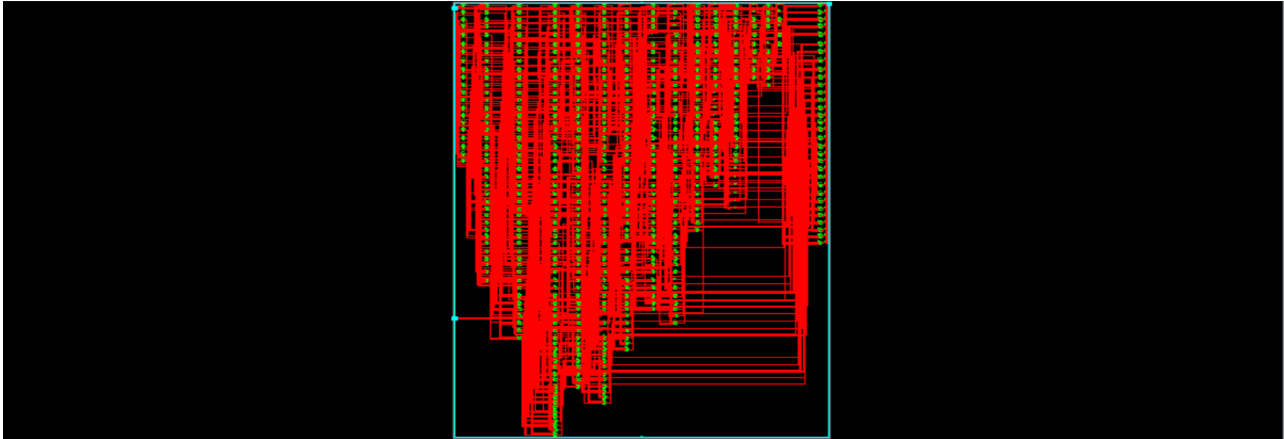


Fig 3 : Technology Schematic result

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Timing Report

NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.
FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT
GENERATED AFTER PLACE-and-ROUTE.

Clock Information:
-----
No clock signals found in this design

Asynchronous Control Signals Information:
-----
No asynchronous control signals found in this design

Timing Summary:
-----
Speed Grade: -2

Minimum period: No path found
Minimum input arrival time before clock: No path found
Maximum output required time after clock: No path found
Maximum combinational path delay: 14.011ns

Timing Details:
-----

```

Fig 4: Timing Summary Result

LUT6:I0->O	2	0.105	0.798	c42/a1/cout1 (cout00<2>)
LUT6:I0->O	2	0.105	0.798	c43/a2/cout1 (c<46>)
LUT6:I0->O	3	0.105	0.611	c6/f4/Mxor_sum_xo<0>1 (c6/s4)
LUT3:I0->O	2	0.105	0.362	c6/f5/cout1 (cout4<7>)
LUT5:I4->O	2	0.105	0.785	c7/f6/Mxor_sum_xo<0>1 (s<49>)
LUT6:I1->O	3	0.105	0.611	h232/cout1 (c<82>)
LUT5:I2->O	3	0.105	0.611	h234/cout1 (c<84>)
LUT5:I2->O	3	0.105	0.611	h236/cout1 (c<86>)
LUT5:I2->O	3	0.105	0.611	h238/cout1 (c<88>)
LUT5:I2->O	3	0.105	0.611	h240/cout1 (c<90>)
LUT5:I2->O	3	0.105	0.611	h242/cout1 (c<92>)
LUT5:I2->O	2	0.105	0.785	h244/cout1 (c<94>)
LUT5:I0->O	3	0.105	0.611	h245/cout1 (c<95>)
LUT5:I2->O	3	0.105	0.611	h247/cout1 (c<97>)
LUT5:I2->O	3	0.105	0.661	h249/cout1 (c<99>)
LUT6:I2->O	3	0.105	0.369	h251/cout1 (c<101>)
LUT5:I4->O	2	0.105	0.798	h253/cout1 (c<103>)
LUT6:I0->O	1	0.105	0.339	h254/Mxor_sum_xo<0>1 (y_30_OBUF)
OBUF:I->O		0.000		y_30_OBUF (y<30>)
Total			14.011ns (1.891ns logic, 12.120ns route)	
			(13.5% logic, 86.5% route)	

Fig 5 : Timing Details Result

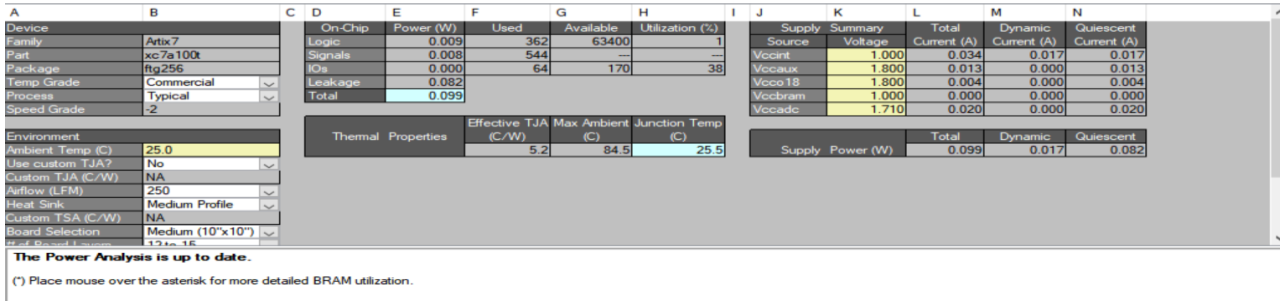


Fig 6: Power supply results

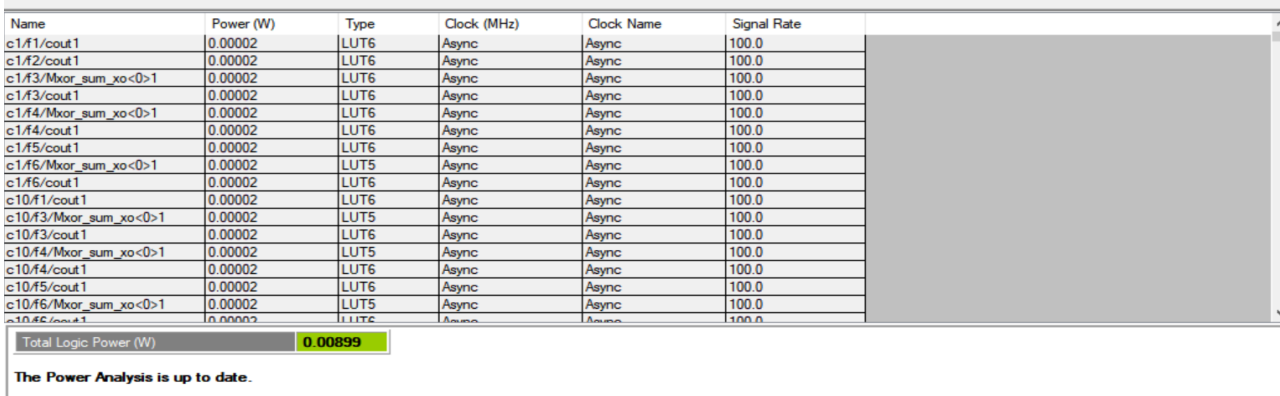


Fig 7 : Logic power Result

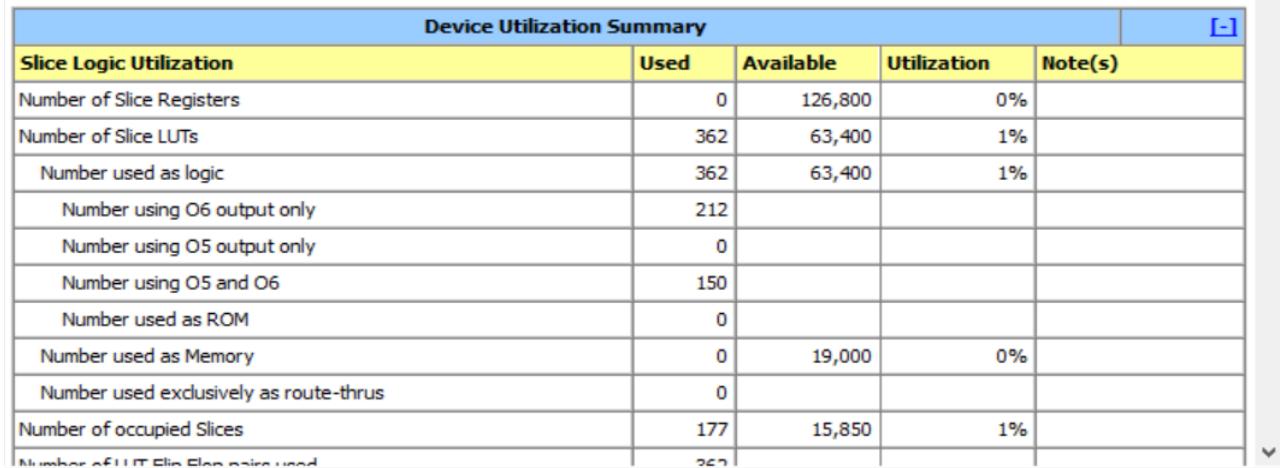
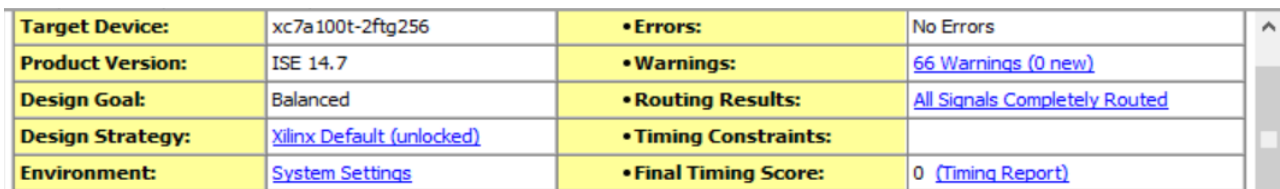


Fig 8: Design Summary

Figures show the results of 16*16 multiplier using 8:2 compressor. Fig1: simulation result of 16*16 multiplier which reduces the bits up to 32 from 256 bits. Fig2: synthesis result which is hardware design using software or Internal structure architecture. Fig3: Technology Schematic with help of LUTs. Fig 4: Timing summary which has speed grade in just 2 steps. Fig 5: Timing details which has Time delay 14.01 ns and 1.891ns for logic delay. Fig 6 & 7 : Power analysis which has 0.09 consumed power and 0.008 logic power. Fig 8: Design Summary.

IV. CONCLUSION

The proposed high-performance, 8:2 high-order compressor-based multiplication architecture represents a significant advancement in digital arithmetic design, addressing the limitations of traditional multipliers. By leveraging high-order compressors, the architecture enhances computational efficiency through reduced propagation delay and minimized hardware complexity. The innovative design processes eight input bits simultaneously, generating two output bits, which significantly decreases the number of summation levels required. Extensive simulations and hardware implementations demonstrate that this architecture outperforms conventional multipliers in terms of speed and power efficiency, achieving notable reductions in dynamic power dissipation and area overhead. The architecture's scalability makes it suitable for integration into various advanced digital systems, including DSPs and AI accelerators. Additionally, the incorporation of power-saving techniques ensures its applicability in low-power environments. Future research directions include exploring higher-order compressors and optimizing designs for emerging technologies. Overall, this architecture sets a new benchmark for high-speed, energy-efficient multiplication solutions in next-generation computing platforms.

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