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Design of AMBA APB Bridge for Two High-Speed Peripheral Communication

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ABSTRACT: The Advanced Microcontroller Bus Architecture (AMBA) Advanced Peripheral Bus (APB) is a widely used low-power, low-complexity bus protocol designed for peripheral devices in system-on-chip (SoC) architectures. This project focuses on the design and verification of an AMBA APB protocol with one master and two slaves using Verilog. The design aims to ensure seamless communication between the master and multiple slave devices while maintaining data integrity and minimizing power consumption. Verification is performed using Verilog to validate the functional correctness of the design. The project employs testbenches and assertions to evaluate performance and compliance with the AMBA APB specification.

KEYWORDS: Pipelined Data, SOC, Synthesis, Simulation, Verilog HDL, Handshaking Signal, AMBA. AMBA APB Bridge, High-Speed Peripheral Communication, System-on-Chip (SoC), Verilog HDL, State Machine-Based Design, FPGA Synthesis, Low-Power Computing

I. INTRODUCTION

The Advanced Microcontroller Bus Architecture (AMBA) is a widely adopted open standard for on-chip communication in System-on-Chip (SoC) designs. Within the AMBA family, the Advanced Peripheral Bus (APB) protocol is specifically tailored for interfacing low-speed peripherals like UARTs, timers, GPIO controllers, and interrupt controllers. APB is designed for simplicity, low power consumption, and low bandwidth, making it ideal for peripherals that do not require high-speed data transfer. It operates synchronously and uses a non-pipelined protocol with distinct address and data phases, ensuring predictable timing and straightforward integration into digital systems. In a typical SoC, high-performance components use buses like AHB (Advanced High-performance Bus) or ASB (Advanced System Bus), while low-performance peripherals are connected via APB. This separation optimizes power and performance across the chip. The design and verification of APB are commonly implemented using Verilog, with testbenches to simulate and validate communication between master and slave devices. APB's structure supports multiple masters and slaves, allowing flexible and scalable system configurations. Each APB transaction spans at least two clock cycles and supports burst transfers, improving data throughput efficiency. As chip complexity increases, verification becomes a major bottleneck, highlighting the need for robust and reusable verification IPs. APB verification IPs are highly configurable, making them easy to integrate into different SoC environments.

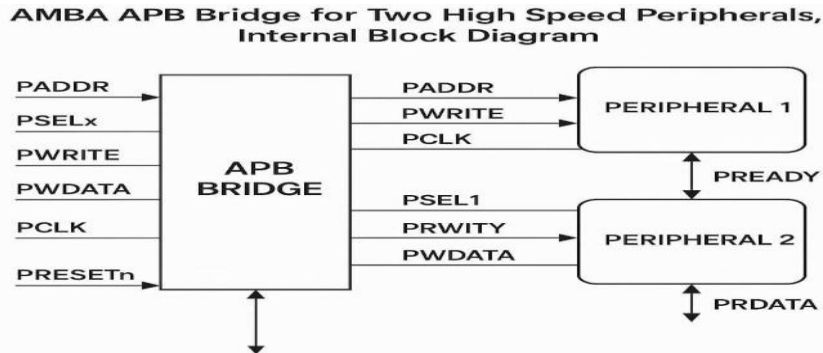
II. PROPOSED SYSTEM

The Advanced Microcontroller Bus Architecture (AMBA), developed by ARM, is a widely used standard for on-chip communication in System-on-Chip (SoC) designs. It enables efficient and reusable integration of various functional blocks like microprocessors, memory, DMA, DSP, and peripherals (UART, USB, I2C, etc.).

AMBA includes several bus protocols:

1. APB (Advanced Peripheral Bus): Used for low-speed, low-power peripherals. It is a non-pipelined, simple protocol ideal for peripherals such as timers, UARTs, and GPIOs. It uses separate address and data phases and supports basic read/write transactions.

- 2. AHB/ASB (Advanced High-performance/System Bus): Used for high-bandwidth components such as memory, DMA, and CPUs. AHB supports burst transfers and multiple masters/slaves.
- 3. AXI (Advanced eXtensible Interface): A high-performance point-to-point protocol introduced in AMBA 3 to overcome the limitations of shared buses. AXI supports pipelining, multiple outstanding transfers, and separate read/write channels



- 4. AXI-lite: A simplified version of AXI without burst support.
- 5. AXI-stream: Optimized for continuous data flow (e.g., video streaming), with no read/write distinction.
- 6. ACE (AXI Coherency Extensions) : Adds cache coherency support for multi-core systems.
- 7. ACE-lite – A simplified ACE for agents without caches but needing coherency.
- 8. CHI (Coherent Hub Interface) : Introduced in AMBA 5, this is a packet-based, scalable protocol for high-

performance, coherent systems with many cores and heterogeneous compute elements.

APB Master and Slave Design

APB Master: Initiates read/write/idle transactions. It works through an APB bridge that:

Latches the address for the entire transaction.

Decodes the address and activates a specific peripheral via a select signal.

Drives write data onto the bus or reads data from the slave.

APB Slave: Has a simple and flexible interface. On the rising clock edge, if select and enable are high:

For write: The register to be updated is determined using the address.

For read: Data is driven onto the bus when the write signal is low.

III. EXPERIMENTAL RESULTS

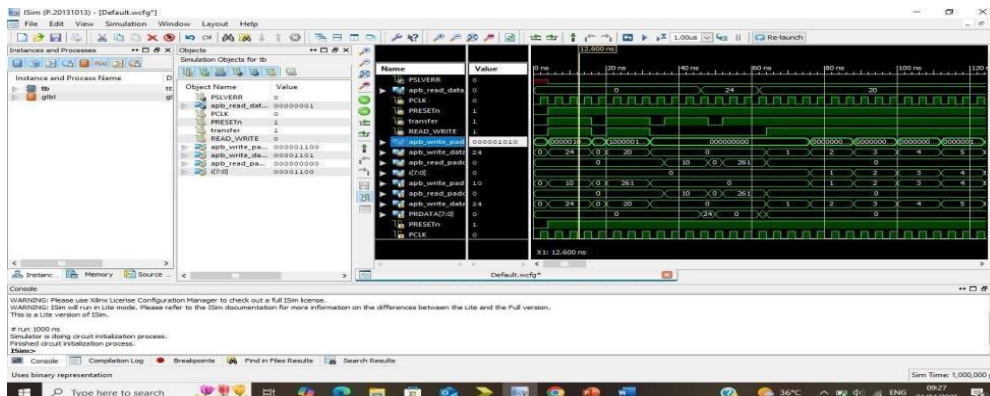


Fig1: Simulation Results

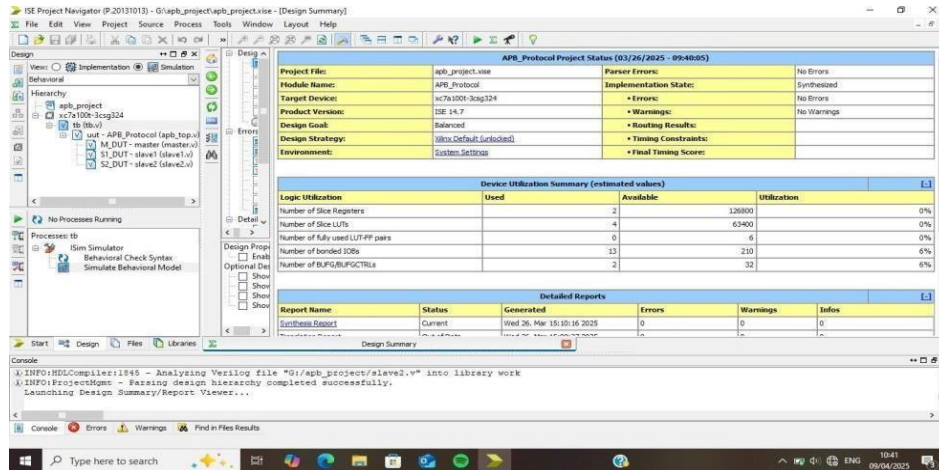


Fig2:Design Summary

IV. CONCLUSION

The design and verification of the AMBA APB protocol with one master and two slaves successfully demonstrate an efficient communication interface for peripheral devices. The use of Verilog for implementation and Verilog for verification ensures a functionally correct and optimized design. The project highlights the protocol's suitability for low-power and cost-effective applications, making it an ideal choice for SoC and embedded system designs

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